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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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TUNG & ASSOCIATES
Suite 120
838 W. Long Lake Road
Bloomfield Hills, MI 48302

EXAMINER	
MANDALA, VICTOR A	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 03/27/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

H·A

Office Action Summary	Application No.	Applicant(s)	
	10/816,413	HO, CHI SHEN	
	Examiner	Art Unit	
	Victor A. Mandala Jr.	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-41* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-38,40 and 41* is/are rejected.

7)☒ Claim(s) *39* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Objections

Claim 39 is objected to because of the following informalities: Claim 39 does not exist in the claim set. Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

Claims 1-8, 11, 14, 19-22, 25, 28, 33-36, & 38 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,825,553 Chua et al.

1. Referring to claim 1, a method of making a semiconductor package comprising: providing a semiconductor chip carrier substrate, (Figure 2 #202), having a first surface and a plurality of cavities, (Figure 2 #205), formed in the first surface and wherein each cavity, (Figure 2 #205), is defined, at least in part, by a bottom surface and at least one sidewall; placing an integrated circuit chip, (Figure 2 #214), having bond pads, (Figure 2 #215), on an upper surface thereof, in each of the cavities, (Figure 2 #205), formed in the chip carrier substrate, (Figure 2 #202), and wherein each semiconductor chip, (Figure 2 #214), overlies the bottom surface; forming a first dielectric layer, (Figure 2 #222), over the first surface of the chip carrier substrate, (Figure 2 #202), and over the integrated circuit chip, (Figure 2 #214), in each of the cavities.

2. Referring to claim 2, a method as set forth in Claim 1 further comprising forming a first set of vias in the first dielectric layer, (Figure 2 #222), and so that each of the first set of vias is aligned with a bond pad, (Figure 2 #215), of the integrated circuit chip, (Figure 2 #214).

3. Referring to claim 3, a method as set forth in Claim 2 further comprising, (Col. 7 Lines 48-50 where the following steps and/or upper layers of Figure 3 are used on the lower layers of Figure 2), forming an electrically conductive traces, (Figure 3 #308), over the first dielectric layer, (Figure 2 #222), and so that each one of the electrically conductive trace, (Figure 3 #308), is electrically is connected to the one of the bond pads, (Figure 2 #215 & Figure 3 area of #306), of the integrated circuit chip, (Figure 2 #214 & Figure 3 #304).

4. Referring to claim 4, a method as set forth in Claim 3 further comprising, (Col. 7 Lines 48-50 where the following steps and/or upper layers of Figure 3 are used on the lower layers of Figure 2), forming a second dielectric layer, (Figure 3 #316), over the redistribution traces, (Figure 3 #308), and forming a second set of vias, (Figure 3 #318), in the second dielectric layer, (Figure 3 #316), so that each of the second set of vias, (Figure 3 #318), communicates, (via #314), with one of the redistribution traces, (Figure 3 #308).

5. Referring to claim 5, a method as set forth in Claim 4 further comprising forming electrically conductive bumps, (Figure 3 #320), wherein each electrically conducted bump, (Figure 3 #320), overlies the second dielectric layer, (Figure 3 #316), and extends into one of the vias, (Figure 3 #318), formed in the second dielectric layer, (Figure 3 #316), and so that the electrically conductive bump, (Figure 3 #320), is electrically connected, (via #314), to one of the redistribution traces, (Figure 3 #308).

6. Referring to claim 6, a method as set forth in Claim 5 further comprising sectioning the semiconductor chip carrier into individual packages each including a semiconductor chip, (Col. 8 Lines 45-60).

7. Referring to claim 7, a method as set forth in Claim 1 wherein the semiconductor chip carrier comprises at least one of silicone, glass, ceramic, and plastic, (Col. 7 Lines 19-20).

8. Referring to claim 8, a method as set forth in Claim 1 wherein the plurality of cavities are formed by etching a semiconductor chip carrier substrate, (Col. 3 Lines 61-63).

9. Referring to claim 11, a method as set forth in Claim 1 further comprising depositing an adhesive, (Figure 2 #216), over the bottom surface defining each cavity, (Figure 2 #205), prior to placing the integrated circuit chip, (Figure 2 #214), in each cavity.

10. Referring to claim 14, a method as set forth in Claim 3 wherein the electrically conductive redistribution traces comprise copper, (Col. 8 Lines 2-4).

11. Referring to claim 19, a method as set forth in Claim 6 wherein the sectioning comprises cutting the chip carrier substrate with a saw, (Col. 8 Line 48).

12. Referring to claim 20, a method of making a semiconductor package comprising: providing a wafer size semiconductor chip carrier substrate, (Figure 2 #202), having a first surface and a plurality of cavities, (Figure 2 #205), formed in the first surface and wherein each cavity, (Figure 2 #205), is defined, at least in part, by a bottom surface and at least one sidewall; placing an integrated circuit chip, (Figure 2 #214), having bond pads, (Figure 2 #215), on an upper surface thereof, in each of the cavities, (Figure 2 #205), formed in the wafer size chip carrier substrate, (Figure 2 #202), and wherein each semiconductor chip, (Figure 2 #214), overlies the bottom surface; forming a first dielectric layer, (Figure 2 #222), over the first surface

of the chip carrier substrate, (Figure 2 #202), and over the integrated circuit chip, (Figure 2 #214), in each of the cavities, (Figure 2 #205); forming a first set of vias, (Figure 2 #224), in the first dielectric layer, (Figure 2 #222), and so that each of the first set of vias, (Figure 2 #224), is aligned with a bond pad, (Figure 2 #215), of the integrated circuit chip, (Figure 2 #214); forming, (Col. 7 Lines 48-50 where the following steps and/or upper layers of Figure 3 are used on the lower layers of Figure 2), an electrically conductive layer over, (Figure 3 #308), the first dielectric layer, (Figure 2 #222), and down into the vias, (Figure 2 #215), formed in the first dielectric layer, (Figure 2 #222), and selectively removing portions, (Col. 7 Lines 66-67), of the electrically conductive layer, (Figure 3 #308), to form electrically conductive traces, (Figure 3 #308), and so that each one of the electrically conductive trace, (Figure 3 #308), is connected to the one of the bond pads, (Figure 2 #215), of the integrated circuit chip, (Figure 2 #214); forming a second dielectric, (Figure 3 #316), over the redistribution traces, (Figure 3 #308), and forming a second set of vias, (Figure 3 #318), in the second dielectric layer, (Figure 3 #316), so that each vias communicates, (via #314), with one of the redistribution traces, (Figure 3 #308); forming electrically conductive bumps, (Figure 3 #320), wherein each electrically conducted bump, (Figure 3 #320), overlies the second dielectric layer, (Figure 3 #316), and extends into one of the vias, (Figure 3 #318), formed in the second dielectric layer, (Figure 3 #3168), and so that the electrically conductive bump, (Figure 3 #320), is electrically connected, (via #314), to one of the redistribution traces, (Figure 3 #308); sectioning the semiconductor chip carrier, (Figure 2 #202), so into individual packages each including a semiconductor chip, (Col. 8 Line 48).

13. Referring to claim 21, a method as set forth in Claim 20 wherein the semiconductor chip carrier, (Figure 2 #202), comprises at least one of silicone, glass, ceramic, and plastic, (Col. 7 Lines 19-20).

14. Referring to claim 22, a method as set forth in Claim 20 wherein the plurality of cavities are formed by etching a semiconductor chip carrier substrate, (Col. 3 Lines 61-63).

15. Referring to claim 25, a method as set forth in Claim 20 further comprising depositing an adhesive, (Figure 2 #216), over the bottom surface defining each cavity, (Figure 2 #205), prior to placing the integrated circuit chip, (Figure 2 #214), in each cavity.

16. Referring to claim 28, a method as set forth in Claim 20 wherein the electrically conductive redistribution traces comprise copper, (Col. 8 Lines 2-4).

17. Referring to claim 33, a method as set forth in Claim 20 wherein the sectioning comprises cutting the chip carrier substrate with a saw, (Col. 8 Line 48).

18. Referring to claim 34, a semiconductor package comprising: a semiconductor chip carrier substrate, (Figure 2 #202), having a first surface and a plurality of cavities, (Figure 2 #205), formed in the first surface and wherein each cavity, (Figure 2 #205), is defined, at least in part, by a bottom surface and at least one sidewall; an integrated circuit chip, (Figure 2 #214), having bond pads, (Figure 2 #215), on an upper surface thereof, in each of the cavities, (Figure 2 #205), formed in the chip carrier substrate, (Figure 2 #202), and wherein each semiconductor chip, (Figure 2 #214), overlies the bottom surface; a first dielectric layer, (Figure 2 #222), over the first surface of the chip carrier substrate, (Figure 2 #202), and over the integrated circuit chip, (Figure 2 #214), in each of the cavities, (Figure 2 #205); a first set of vias, (Figure 2 #224), in the first dielectric layer, (Figure 2 #222), and so that each vias is aligned with a bond pad, (Figure 2

#215), of the integrated circuit chip, (Figure 2 #214); & (Col. 7 Lines 48-50 where the following steps and/or upper layers of Figure 3 are used on the lower layers of Figure 2),an electrically conductive traces over the first dielectric layer, (Figure 2 #222), and one of the traces extending down into the one of the vias, (Figure 2 #224), formed in the first dielectric layer, (Figure 2 #222), so that each one of the electrically conductive trace is electrically is connected to the one of the bond pads, (Figure 2 #215), of the integrated circuit chip, (Figure 2 #214); a second dielectric layer, (Figure 3 #316), over the redistribution traces, (Figure 3 #308), and a second set of vias, (Figure 3 #318), in the second dielectric layer, (Figure 3 #316), so that each vias communicates, (via #314), with one of the redistribution traces, (Figure 3 #308); electrically conductive bumps, (Figure 3 #320), wherein each electrically conducted bump, (Figure 3 #320), overlies the second dielectric layer, (Figure 3 #316), and extends into one of the vias, (Figure 3 #318), formed in the second dielectric layer, (Figure 3 #316), and so that the electrically conductive bump, (Figure 3 #320), is electrically connected, (via #314), to one of the redistribution traces, (Figure 3 #308).

19. Referring to claim 35, a semiconductor package as set forth in Claim 34 wherein the semiconductor chip carrier comprises at least one of silicone, glass, ceramic, and plastic, (Col. 7 Lines 19-20).

20. Referring to claim 36, a semiconductor package as set forth in Claim 34 further comprising an adhesive, (Figure 2 #216), over the bottom surface defining each cavity, (Figure 2 #205), and underlying the integrated circuit chip, (Figure 2 #214), in each cavity.

21. Referring to claim 38, a semiconductor package as set forth in Claim 34 wherein the electrically conductive redistribution traces comprise copper, (Col. 8 Lines 2-4).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 13, 16, 18, 27, 30, 32, 37, and 41 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,825,553 Chua et al.

22. Referring to claim 13, a method as set forth in Claim 1 wherein the first dielectric layer comprises at least one of a polyimide and BCB, (Col. 5 Lines 61-62).

Chua et al. discloses the claimed invention but is silent on the exact material used for the first and second dielectric layers, but teaches the material dielectric material used in the first embodiment to be a polyimide in Col. 5 Lines 61-62. It would have been obvious to one having ordinary skill in the art at the time the invention was made to make the first and second dielectric layers out of a polyimide, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice.

In re Leshin, 125 USPQ 416.

23. Referring to claim 16, a method as set forth in Claim 4 wherein the second dielectric layer comprises at least one of a polyimide and BCB, (Col. 5 Lines 61-62 and See ** above).

24. Referring to claim 27, a method as set forth in Claim 20 wherein the first dielectric layer comprises at least one of a polyimide and BCB, (Col. 5 Lines 61-62 and See ** above).

25. Referring to claim 30, a method as set forth in Claim 20 wherein the second dielectric layer comprises at least one of a polyimide and BCB, (Col. 5 Lines 61-62 and See ** above).

26. Referring to claim 37, a semiconductor package as set forth in Claim 34 wherein the first dielectric layer comprises at least one of a polyimide and BCB, (Col. 5 Lines 61-62 and See ** above).

27. Referring to claim 41, a semiconductor package as set forth in Claim 34 wherein the second dielectric layer comprises at least one of a polyimide and BCB, (Col. 5 Lines 61-62 and See ** above).

28. Referring to claim 18, a method as set forth in Claim 5 wherein the electrically conductive bumps are formed by at least one of ball placement, (Col. 2 Line 7 and See */* below), stenciling, and plating.

/ Chua et al. teaches all of the claimed matter in claim 18 and 32, but is silent on the exact process used to put the bumps on the device, but does teach ball placement in another embodiment in Col. 2 Line 7. It would have been obvious to one having skill in the art at the time the invention was made to use ball placement as a processing step because it is a known process, which lacks an inventive step.

29. Referring to claim 32, a method as set forth in Claim 20 wherein the electrically conductive bumps are formed by at least one of ball placement, (Col. 2 Line 7 and See */* above), printing, and plating.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 15, 29, and 40 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,825,553 Chua et al. in view of U.S. Patent No. 6,617,674 Becker et al.

30. Referring to claim 15, a method as set forth in Claim 14 wherein the electrically conductive redistribution traces further comprise nickel, (Becker et al. Col. 9 Lines 25-28 and See *** below).

*** Chua et al. discloses the claimed invention except for the traces being also made with nickel, but Becker et al. does in Col. 9 Lines 25-28. It would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the teachings of Chua et al. with the teachings of Becker et al. because adding nickel to the copper traces provides a diffusion barrier to the traces, (Becker et al. col. 9 Lines 25-28), and since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice.

In re Leshin, 125 USPQ 416.

31. Referring to claim 29, a method as set forth in Claim 28 wherein the electrically conductive redistribution traces further comprise nickel, (Becker et al. Col. 9 Lines 25-28 and See *** above).

32. Referring to claim 40, a semiconductor package as set forth in Claim 38 wherein the electrically conductive redistribution traces further comprise nickel, (Becker et al. Col. 9 Lines 25-28 and See *** above).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 9, 10, 23, and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,825,553 Chua et al. in view of U.S. Patent No. 6,548,895 Benavides et al.

33. Referring to claim 9, a method as set forth in Claim 1 wherein the cavities are formed by molding the semiconductor circuit chip carrier substrate to provide the cavities, (Benavides et al. Col. 10 Lines 33-35 and See **/* below).

**/* Chua et al. teaches all of the claimed matter in claims 9, 10, 23, & 24, but is silent on the process of forming the cavity in a carrier by molding or milling, but Benavides et al. does in Col. 10 Lines 33-35. It would have been obvious to one having skill in the art at the time the invention was made to make a cavity by a mold process or by a milling process. These processes are known equivalents to an etching process as taught by Chua et al. in Col. 3 Lines 61-63, and where this alternative lacks an inventive step.

34. Referring to claim 10, a method as set forth in Claim 1 wherein the cavities are provided by milling a flat surface of a semiconductor chip carrier substrate, (Benavides et al. Col. 10 Lines 33-35 and See **/* above).

35. Referring to claim 23, a method as set forth in Claim 20 wherein the cavities are formed by molding the semiconductor circuit chip carrier substrate to provide the cavities, (Benavides et al. Col. 10 Lines 33-35 and See **/* above).

36. Referring to claim 24, a method as set forth in Claim 20 wherein the cavities are provided by milling a flat surface of a semiconductor chip carrier substrate, (Benavides et al. Col. 10 Lines 33-35 and See **/* above).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 9, 10, 23, and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,825,553 Chua et al. in view of U.S. Patent No. 5,106,461 Volfson et al.

37. Referring to claim 12, a method as set forth in Claim 2 wherein the first set of vias formed in the first dielectric layer are formed by reactive ion etching, (Volfson et al. Col. 8 Lines 4-8 and See **** below).

**** Chua et al. teaches all of the claimed matter in claims 12, 17, 26, and 31 but is silent in the respect of teaching the narrowed process of ion etching being used to form a via. Chua et al.

teaches etching the dielectric layer to form a via in Col. 8 Lines 15-16. Volfson et al. does teach the process of forming a via by the narrowed technique of ion etching in Col. 8 Lines 4-8. It would have been obvious tone having skill in the art to use the narrowed ion etching process to form a via and where these processes are known equivalents, and where this alternative lacks an inventive step.

38. Referring to claim 17, a method as set forth in Claim 4 wherein the second set of vias is formed in the second dielectric layer by reactive ion etching, (Volfson et al. Col. 8 Lines 4-8 and See **** above).

39. Referring to claim 26, a method as set forth in Claim 21 wherein the first set of vias formed in the first dielectric layer are formed by reactive ion etching, (Volfson et al. Col. 8 Lines 4-8 and See **** above).

40. Referring to claim 31, a method as set forth in Claim 20 wherein the second set of vias is formed in the second dielectric layer by reactive ion etching, (Volfson et al. Col. 8 Lines 4-8 and See **** above).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Victor A. Mandala Jr. whose telephone number is (571) 272-1918. The examiner can normally be reached on Monday through Thursday from 8am till 6pm..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J. Flynn can be reached on (571) 272-1915. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

VAMJ
3/14/06

EVAN PERT
PRIMARY EXAMINER